REMARKS

A new Specification has been filed as part of this Continuation. It includes all the amendments approved and entered in the parent case, and no others, save that the chain of co-pendency required by 35 USC 120 has been added as well.

A new set of Formal Drawings has also been submitted herewith. It also includes corrections that have previously been approved, and includes no other changes.

It is therefore believed that the Specification and Drawings in this new case are free from error and that they contain no new matter whatsoever.

As an aid in citing locations in a reference, let us adopt the following notational convention: lines 4 through 23 in col. 7 of Reichert are referred to as Reichert @ 7:4 - 23. When it is clear that Reichert is the reference under consideration, we can simply say 7:4 - 23, and if only line 10 is needed, 2:10. Also, Reichert @ 7:4 - 8:41 will be appreciated as indicating line 4 of col. 7 through line 41 of col. 8.

Turning now to the action on the merits, and the issues concerning the Drawing, Specification and Claims, we shall now respond to the Final Office Action of 10 July 2003.

Claims 4 - 7 were finally rejected under 35 USC 103 over Reichert (US 6,389,525 B1) and Chen (US 6,018,817). Those claims have been canceled in favor of new claims 8, 9 and 10. Claim 7 has been re-introduced as claim 8, and also has a correction of a misspelled word ("per-defined" should have been --pre-defined--). The rejection of claim 7 (now present as claim 8) is traversed below.

Claim 8 recites the presence of Q-many latches. These latches serve as memory to allow accumulation of the various individually received sub-vectors before the entire reassembled vector is passed on for further processing. The portion of Reichert that performs the corresponding function is his COMPARE CIRCUITRY 26 in Figure 2. He never expands on that block, as the bulk of his disclosure is directed to an expansion of the PATTERN GENERATOR 30. He says very little about the compare process, and though he sends a serial sequence of <address> <data> <data> ... <data> that was the basis for applicants' stipulation that Reichert serializes, that in no way means that the <address> <data> <data> ... <data> are sub-vectors and that he ever re-assembles the receive results into a large sequence to be treated as a unit. It is believed that he writes using a <address> <data> <data> ... <data> sequence, and then simply later repeats the sequence generation activity with the DUT's WRITE control lines changed to READ, and has the COMPARE CIRCUITRY 26 check the newly regenerated <address> <data> <data> ... <data> sequence against the received <address> <data> <data> ... <data> sequence. Each <addr/data> element of each sequence is compared against its counterpart in the other sequence, without bothering to accumulate the entire sequence into a unit. Such a manner of operation is the conventional one, and he never says otherwise. It appears that all he does say is found at 1:25 - 28 and 4:15 - 19. He never discloses or discusses the accumulation of sub-vectors, nor the use of latches to do so. But that is what is claimed in claim 8.

Furthermore, the MUX's 168 - 172 that he shows in Figure 2 are located in the PATTERN GENERATOR 30, and appear to select between issuing <address> or <data>, while upstream MUX 140 joins smaller streams of data into larger ones to allow staggered collections of data generators to run slower than one unified data generator would have to run. None of this involves the claimed latches, and it does not correspond to the claimed sub-vectors, since the various <data> are never sent to the DUT in less than whole <data> units.

Turning now to claim 9, it is directed to a combined mapping and serialization mechanism that is accomplished through one set of n-many MUX's controlled by a memory. Claim 9 recites a structure that has one set of Q-many MUX's controlled by a memory. The one set of MUX's is, under the control of the memory, capable of performing the alteration of an original transmit vector ...

> "...the alteration constituting one of: (a) a mapped transmit vector whose Q-many bits are re-ordered according to a mapping defined by the addressed set of control signal values; or (b) a sequential collection of non-re-ordered signals, each collection being one of a plurality of transmit sub-vectors each having less than Q-many bits and the sequence of the collections being according to a serialization defined by the addressed set of control signal values; or (c) a sequential collection of re-ordered signals, each collection being one of a plurality of transmit sub-vectors each having less than Q-many bits that have also been re-ordered according to a mapping defined by the addresses set of control signal values, and the sequence of the collections being according to a serialization defined by the addressed set of control signal values; and
>
> a programmatically controlled address applied to the memory and that selects a pre-defined alteration stored in the memory and that is to be performed upon the original transmit vector."

The recited language says that the Q-many MUX's, under the control of the memory, can do (a), (b) or (c), where (a) is mapping, (b) is serialization, and (c) is both at the same time.

Reichert does not have a single set of MUX's that can do (a), (b) and (c). Instead, it appears that the MUX's 168 - 172 in Reichert can perform mapping, but they do not serialize by making a transmit vector into a sequence of sub-vectors. Reichert simply sends separate <addr/data> vectors.

Similar argument apply for claim 10, which pertains to the reverse direction of operation, plus it also recites the latches, which, as we have seen are not shown in Reichert.

As for Chen, it appears that this patent deals with error correcting codes in a memory system, and we are still unable to find anything in it that combines with Reichert to suggest the claimed structures in a memory tester for serialization and mapping of transmit vectors and for de-serialization and reverse mapping.

Thus, on the basis of the explanation and arguments set out above, Claims 7 - 9 are believed to comply with 35 USC 103, and the Examiner is respectfully, but earnestly, urged to withdraw the rejections.

THEREFORE, further examination is requested, and favorable action is respectfully solicited.

Respectfully submitted,
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